Innovative strategies for the design of clock networks in nanometer technologies
To improve the speed (clock frequency), dimensional scaling is supported by the reduction of the number of logic stages (logic depth) inside each pipeline stage.

Increasing impact of clocked storage elements (CSEs) timing on the cycle time.

Timing targets of CSEs:

1) Minimize the overall delay: \( \min(t_{\text{setup}} + T_{CQ}) = T_{DQ,\text{opt}} \)

2) Provide soft-clock-edge features when dealing with critical paths (to absorb clock uncertainties and allow time-borrowing)

3) Achieve positive race immunity \( R = T_{CQ} - t_{\text{hold}} \) values when dealing with fast paths
The impact of the clock network on the performances of VLSI microprocessors (2)

The nonscaling of device subthreshold characteristics and the growing impact of gate leakage led to a deviation of the actual scaling scenarios from the constant-field scaling. Hence, power becomes the major concern and nowadays VLSI systems undergo “power-limited” scaling, thus implying the necessity of:

1) Changes in chip architecture and new design strategies/techniques
2) Energy-efficiency achievement
3) Use of multiple devices with different features

Clock network (made up by generation and distribution circuits and by the clocked storage elements) dissipates a large fraction of the whole chip energy budget.

Up to 30-50% of the total power in HP µPs.
Main research objectives

1) Search for new efficient design approaches at the clock-domain level and optimization of the clock network design through the clock slope setting.

2) Development of suitable design/optimization strategies to achieve energy-efficient solutions in the Energy-Delay (E-D) design space (not only for CSEs).

3) Study of the impact of leakage and variability sources, which primarily affect the performances of nanometer circuits. Effectiveness of leakage/variability reduction techniques and search for new ones.

4) Development of novel CSE circuit topologies to improve the energy-delay tradeoff in pipelined systems.

Secondary and related targets

1) Device-level modelization of I-V characteristics and of the “layout impact” (i.e., the impact of local interconnections).

2) Study on the effect of the intradie/interdie variations on digital circuits and on the procedures to correctly evaluate the evolution of these impacts.
Clock slope optimization at the clock-domain level: characterization of CSEs

To define possible tradeoffs at the clock-domain level concerning the adopted clock slope, a preliminary study of the slope impact on CSEs performances is necessary.

Definition of a proper testbench

CSE under test
Parasitics due to local data, clock and internal wires
Driving circuitry to achieve the desired slope

\[ C_x = \sum_{i} w_i \left( C_i - C_p - C_v \right) \]

FOX slope
Layout impact included in the optimization carried out to achieve minimum ED^3, ED and E^3D designs.

C_{par-clk}
To achieve generality of results, the study is carried out on several CSE classes (4) and topologies (15)
Clock slope influence on CSEs energy, delay and race immunity

The clock distribution stages are usually oversized to ensure steep clock waveforms (typically FO2-FO3 slope) in order to avoid speed-energy penalties in the CSEs.

The analysis carried out on CSEs reveals that:

- $\tau_{\text{DQ, opt}}$ is substantially not affected for FO2-FO6 slope (especially for Pulsed CSEs)
- Energy increases almost linearly (magnified current contentions) $\rightarrow E_{\text{CSE}} = kX + q$
- $R = \tau_{\text{CQ}} t_{\text{hold}}$ slightly increases for all topologies (better race immunity)
Overall clock domain energy consumption and optimum network design: analysis (1)

On the contrary, a smooth clock slope allows for downsizing of local clock domain buffers (the ratio $V_{DD}/V_{TH}$ is low in nanometer technologies).

Hence, an energy tradeoff arises

Buffers load is made up by the clock capacitance of each clock-driven CSE and by the wires distributing the clock throughout the domain.

$$C_L = M \left( \frac{C_i}{n^3} \sum_{i} w_i + C_p \right) + c_M (\sqrt{M} + 2)L_d$$

- $M$: number of CSEs in a clock domain
- The domain clock wires are supposed in Metal5, with CSEs uniformly distributed in a square domain with side $L_{dom}$ and a pseudo grid-serpentine distribution scheme
Overall clock domain energy consumption and optimum network design: analysis (2)

The energy consumption of local buffers is made up by dynamic, static (leakage) and short-circuit contributions and has to be evaluated versus the clock slope $X$:

$$E_{buf} = \left( \frac{2}{1 - X} \right) \left( \frac{1 - X^N}{1 - X} \right) V_D^2 \left( T_C \frac{V_D}{V} \left( 1 - X^N \right) \right) [a + b(X - 2)]$$

- **$V_{DD}$**: supply voltage
- **$T_{CK}$**: clock period
- **$N$**: number of stages

$E_{buf}$ strongly decreases with $X$ and hence a tradeoff arises with the energy of the CSEs $\rightarrow ME_{CSE}$. The optimum clock slope from as concerns clock domain consumption is:

$$X_o = 1 + \sqrt{\left( a - b \right) \left( \frac{2}{V} \right) \left( \frac{T_C}{V} \right) \left( I_L \right)}$$

$$\left( 1 - \frac{C_i}{V} \sum w_i \frac{C_p}{V} + \frac{C_m}{V} \left( \sqrt{M + 2} \right) \frac{L_D}{V} \right) - j$$
Overall clock domain energy consumption and optimum network design: results (1)

\( X_{\text{opt}} \) mainly depends on \( k \), \( M \) and on the overall clock input capacitance of a CSE (i.e. also on the specific CSE design)

Optimum clock slope can significantly depart from typically adopted values (\( X=2 \), \( X=3 \)). \( X_{\text{opt}} \) increases:

1) when \( M \) is low (significantly)
2) when designing for low-power instead of high-speed, i.e. for smaller CSEs sizings (slightly)
3) when the clock load brought by each CSE increases (slightly)
Optimum clock slope typically lies in the range FO4-FO6 and is significantly smooth for DET and Pulsed topologies. It can lead up to 40% (235%) energy savings compared with FO3 (FO2) approach at the cost of minor or no speed degradation.
Clock skew and jitter are fundamental specifications since their impact has to be budgeted in the cycle time requirement. Supply variations, capacitive crosstalk and intradie variations at the clock-domain level are accounted for when the clock slope is varied in the range FO2-FO6.

At the clock-domain level, intradie variations and capacitive crosstalk are nearly not affected by clock slope (skew-jitter incrementes smaller than 0.1 FO4 delay). At this scale, supply noise is even reduced because it is proportional to the reduced overall delay of buffers, which is reduced.
In the FO2-FO6 slope range, also the variability of $\tau_{DQ,opt}$ is practically unchanged.

$\tau_{CQ}$ delay suffers slightly greater increments than $\tau_{DQ,opt}$ (no more than 18%), while its variability raises up to 11% for FO6 clock slope.

The suggested relaxation in the local clock network design cannot turn fast paths into critical paths (supported by the trend of the race immunity $R = \tau_{CQ} - t_{\text{hold}}$, which even raises with smoother clock slopes).

Summarizing, such an optimization brings significant advantages in terms of energy dissipation while maintaining speed performances substantially unaffected and without worsening local skew-jitter and variability of CSEs.
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